AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A method for fabricating a semiconductor transistor, comprising:

forming a first insulating layer on a semiconductor substrate;

forming an LDD region using ion implantation;

patterning the first insulating layer;

forming a trench in the substrate after forming the LDD region;

forming a trench gate by depositing and planarizing a second insulating layer and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor;

forming a photoresist pattern on the substrate;

forming source/drain regions by performing an ion implantation using the photoresist pattern as a mask; and

removing the photoresist pattern and the first insulating layer.

2. (original) The method of claim 1, further comprising performing a thermal process after removing the first insulating layer.

3. (original) The method of claim 1, wherein the first insulating layer works as a buffer layer during the ion implantation for forming the LDD and the source/drain regions.

4. (original) The method of claim 1, wherein the first insulating layer is made of one selected from the group consisting of nitrides, tantalum oxides, titanium oxides, and hafnium oxides.

5. (original) The method of claim 1, wherein the conductor is made of one selected from the group consisting of tungsten alloys, titanium alloys, and tantalum alloys.

6. (original) The method of claim 1, wherein the energy of the ion implantation for forming the LDD region is between 30 keV and 80 keV.

7. (original) The method of claim 1, wherein the energy of the ion implantation for forming the source/drain regions is between 5 keV and 60 keV.

8. (original) The method of claim 1, wherein the trench is formed by a dry etching with an etching angle between 5° and 30°.

9. (original) The method as defined by claim 1, wherein the trench is formed using chemical dry etching.

10. (original) The method as defined by claim 9, wherein lower edges of the trench are formed in a rounded shape.

11. (original) The method of claim 1, wherein planarizing the second insulating layer and the conductor comprises a CMP process using the first insulating layer as an etch-stop layer.

12. (original) The method of claim 1, wherein the first insulating layer is removed by a wet etching using a phosphoric acid solution.

13. (previously presented) A method for fabricating a semiconductor transistor, comprising:

forming an LDD region using an ion implantation in a substrate;

forming a first insulating layer on the substrate;

patterning the first insulating layer;

forming a trench in the substrate;

forming a trench gate by depositing and planarizing a second insulating layer and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor;

anisotropically etching the first insulating layer to form spacers; and

forming source/drain regions by performing an ion implantation on the substrate using the spacers and the trench gate as a mask.

14. (original) The method of claim 13, further comprising performing a thermal process after forming the source/drain regions.

15. (original) The method of claim 13, wherein the first insulating layer is an oxide layer or a nitride layer.

16. (original) The method of claim 13, wherein the conductor comprises one selected from the group consisting of polysilicon, tungsten alloys, titanium alloys, and tantalum alloys.

17. (original) The method of claim 13, wherein the energy of the ion implantation for forming the LDD region is between 10 keV and 80 keV.

18. (original) The method of claim 13, wherein the energy of the ion implantation for forming the source/drain regions is between 10 keV and 100 keV.

19. (original) The method of claim 13, wherein the trench is formed by dry etching.

20. (original) The method of claim 13, wherein the trench is formed by a dry etching using an angle etching and chemical dry etching.

21. (original) The method of claim 20, wherein lower edges of the trench are formed in a rounded shape.

22. (original) The method of claim 20, wherein the chemical dry etching uses CF_4/O_2 or CHF_3/O_2.

23. (original) The method of claim 13, wherein planarizing a second insulating layer and a conductor comprises a CMP process using the first insulating layer as an etch-stop layer.

24. (currently amended) A method for fabricating a semiconductor transistor, comprising:

depositing a first insulating layer on a semiconductor substrate;

forming an LDD region using an ion implantation;

patterning the first insulating layer;

forming a trench in the substrate after forming the LDD region;

forming a trench gate by depositing and planarizing a second insulating layer and a first conductor on the substrate with the trench, the trench gate comprising the second insulating layer and the conductor;

depositing a second conductor on the substrate with the trench gate formed thereon;

patterning the second conductor and the first insulating layer; and

forming source/drain regions by performing an ion implantation using the patterned second conductor as a mask.

25. (original) The method of claim 24, wherein the first insulating layer works as a buffer layer during the ion implantation for forming the LDD region.

26. (original) The method of claim 24, wherein the first insulating layer is a nitride layer.

27. (original) The method of claim 24, wherein the first conductor is made of polysilicon and the second conductor is made of one selected from the group consisting of tungsten alloys, titanium alloys, and tantalum alloys.

28. (original) The method of claim 24, wherein the energy of the ion implantation for forming the LDD region is between 5 keV and 60 keV.

29. (original) The method of claim 24, wherein the energy of the ion implantation for forming the source/drain regions is between 30 keV and 80 keV.

30. (original) The method of claim 24, wherein planarizing a second insulating layer and a first conductor comprises a CMP process.

31. (original) The method of claim 30, wherein the CMP process uses the first insulating layer as an etch-stop layer.